REMARKS

Claims 1-13 are pending in the application. Claims 12 and 13 stand rejected provisionally under 35 U.S.C. §101 for double patenting as claiming the same invention as claims of 7 and 8 copending patent application 10/435,626 (the Copending Patent Application). Claims 6-11 stand rejected provisionally on nonstatutory double patenting as unpatentable over claims 1-6 of the Copending Patent Application in view of three prior art references: United States Patent Number 4,670,882 to Hosaka et al (Hosaka); United States Patent Number 5,345,583 to Davis; and United States Patent Number 5,822,515 to Baylocq. Claims 6-10 stand rejected under 35 U.S.C. §112 due to the recitation of "the VLIW microprocessor" without an antecedent. Objections are made to Claims 6, 8 and 11 due to informal recitations. Claim 10 is provisionally objected to as being a substantial duplicate of claim 6.

As to rejections on prior art, Claim 12 is rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent Number 4,670,882 to Jitsukawa et al (Jitsukawa). Claims 12 and 13 are rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent Application Publication Number 2004/0153747, which corresponds to the Copending Patent Application. Claims 1-5 and claims 6-11 stand rejected under 35 U.S.C. §103(a) on Czajkowski, the Copending Patent Application, in view of Hosaka, in view of Davis and further in view of Baylocq.

Applicants have canceled claims 12 and 13 in order to avoid a provisional statutory double patenting rejection in the Copending Patent Application. In response to the present Official Action, Applicants traverse the provisional nonstatutory double patenting rejection of claims 6-11. Formal corrections are made to obviate the rejection under 35 U.S.C. §112 and the objections to the specifications. Further formal corrections are also made. Applicants traverse all rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a).

Statutory Double Patenting Rejection of Claims 12 and 13 - Priority

Claims 12 and 13 stand rejected provisionally under 35 U.S.C. §101 for double patenting as claiming the same invention as claims 7 and 8 of the Copending Patent Application. The Examiner has required a statement of which entity is the prior inventor of conflicting subject matter in this application and the Copending Patent Application. In order to avoid a holding of abandonment, Assignee states that the entity in the Copending Patent Application is a prior inventor with respect to the entity in the present application.

Statutory Double Patenting Rejection of Claims 12 and 13 – Subject Matter

Claims 12 and 13 stand rejected provisionally under 35 U.S.C. §101 for double patenting as claiming the same invention as claims 7 and 8 of the Copending Patent Application. Claims 12 and 13 of the instant application are canceled. Under MPEP 804.02, a statutory double patenting rejection, "is avoided

by canceling the [rejected] claims in all but one of the pending applications." The Copending Patent Application constitutes "all but one of the pending applications," and the recitations in question have been canceled in all other applications referred to under this ground of rejection, i.e., the present application. Therefore, it is submitted that this ground of rejection is avoided in the present application and should be withdrawn in the Copending Patent Application.

Overview of the Preferred Embodiments

Applicants point out in paragraph [0003] that a number of solutions have been developed to correct for or avoid generation of erroneous changes of internal data bits due to single event upsets (SEUs) or single event functional interrupts (SEFIs), also known as environmentally induced hangs. One solution in the prior art is using radiation hardened microprocessors manufactured to be tolerant to radiation. However, radiation hardened microprocessors historically lag commercial devices by two or three generations. For example, at the time of filing of the application, radiation tolerant microprocessors were being produced with 0.35 micron geometries while non-radiation tolerant devices had advanced to 0.13 micron geometries. Larger geometries have slower performance and higher power requirements than smaller geometries.

Embodiments of the present invention use a hardened core circuit which is separate from the microprocessor to control reset and interrupt lines. However,

as explained in paragraph [0017], for example, any microprocessor may be used. Thus the effects of SEUs and SEFIs may be mitigated in an embodiment in which only the core is necessarily hardened. The microprocessor is not required to be hardened.

This is particularly significant in terms of cost of the circuitry used to produce embodiments. A nominal core for use in an embodiment may comprise 5,000 to 10,000 gates. A state of the art microprocessor could contain 50,000,000 transistors nominally comprising 12,000,000 gates. The cost of a hardened core is significantly less than the cost of a hardened microprocessor. As explained below, the recitations of the claims necessarily result in providing the ability to use a commercial (non-hardened) microprocessor, while avoiding SEUs and SEFIs.

The art of record neither discloses in teachings in individual references nor suggests, taking in the references in combination, the structure recited by Applicants. The art of record does not disclose apparatus having the performance characteristics achievable with apparatus made in accordance with Applicants' recitations.

As further described below, specific recitations in Applicants' claims recite structure which will of necessity provide for the above-described advantages. In order to render the claims even more explicit, all claims, whether directly or

through dependency, have been amended to recite a microprocessor "not required to be radiation hardened." This recitation is supported in the specification at paragraph [0017] which states, "The Hardened Core system disclosed herein is a fault detection and correction system capable of being implemented with any microprocessor."

Overview of the Recitations of Claims

Claims 1-5 and claims 6-11 recite a computer system with improved tolerance to functional interrupts. Claims 6-11 further recite fault tolerance in the context of fault tolerance from microprocessor data errors.

Claim 1 recites a computer system with improved tolerance to microprocessor functional interrupts induced by environmental sources. Claims 2-5 are dependent on claim 1 and distinguish over the prior art by virtue of their dependence on claim 1 as well as by their further recitations. Claim 6 recites a computer system with improved fault tolerance from microprocessor data errors. Claims 7-10 are dependent on claim 6 and distinguish over the prior art by virtue of their dependence on claim 6 as well as by their further recitations. Claim 11 is an independent claim reciting a software and hardware computer system with improved fault tolerance from microprocessor data errors and functional interrupts. Claims 1, 6 and claim 11 have certain distinguishing limitations in common.

Claims 1, 6 and 11 each recite a hardened core circuit configured to read a predetermined time or signal from a microprocessor and to activate the microprocessor's interrupt and reset control signals if a timer signal is not received within a predetermined time period to provide for removal of the microprocessor from a functionally interrupted state. A software routine located at the microprocessor's interrupt or reset vector address is configured to restart the microprocessor's application software.

Paragraph [0005] of the present application states in part, "The present application discloses fault tolerant circuits and companion software routines for use in computer systems and method of use. ... [A] fault tolerant software maintenance routine configured to send a periodic output signal from the microprocessor to a separate circuit (termed a "Hardened Core" or "H-Core") in communication with the microprocessor, the Hardened Core circuit configured to monitor the periodic signal, the control lines (reset, non-maskable interrupt, interrupts, etc.) of the microprocessor wired through the Hardened Core circuit in a manner that allows the Hardened Core to selectively and sequentially activate each control line when periodic signal from microprocessor is not received on periodic schedule ..."

The claims recite the structure that enables this performance. For example, recitations in beginning at claim 1, line 4, claim 6, line 18 and claim 11, line 20 each include the hardened core being connected to the microprocessor to respond to

signals from the microprocessor and to provide status, interrupt output and power cycle output signals to the microprocessor. The microprocessor sends predetermined timer signals to the hardened core circuit. As further recited in each claim, the hardened core circuit is configured to read the timer signals. These recitations begin at claim 1, line 12, claim 6, line 21 and claim 11, line 28. If the timer signal is not received within a predetermined time, the hardened core circuit will activate the microprocessor's interrupt and research control input signals. Finally, the claims each recite a microprocessor software routine located at the microprocessor's interrupt or reset vector addresses and which is configured to restart the microprocessor's application software.

As recited in claim 1, lines 9-12, claim 6, lines 19-21 and claim 11, lines 25-27 the timer signal is provided from the microprocessor to the hardened core circuit is connected to the microprocessor and is configured to read the timer signal from the microprocessor.

Non-Statutory Double Patent Rejection of Claims 6-11 and The Rejection of Claims 1-11 Under 35 U.S.C. §103(a)

These rejections are treated together, since they both rely on the same combinations of the same references. Claims 1-5 and claims 6-11 stand rejected under 35 U.S.C. §103(a) on Czajkowski, the Copending Patent Application, in view of Hosaka, in view of Davis and further in view of Baylocq. Claims 6-11 stand

rejected provisionally on the ground of non-statutory "obviousness" double patenting as being unpatentable over claims 1-6 of the Copending Patent Application in view of Hosaka, in view of Davis and further in view of Baylocq. The rejections take the position that, "The copending application discloses, in copending claims 1-6 all the limitations of claims 6-11, except for those involving the hardened core circuit, timer signal resets, and timer initiated interrupts and resets."

Briefly paraphrasing combinations proposed by the rejection, Hosaka proposes a watchdog timer and a core. Additionally, Hosaka discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the hardened core circuit on a predetermined time period. The rejection states that it would have been obvious to one skilled in the art to include the watchdog timer of Hosaka in the invention of Czajkowski and that this would have been obvious because Czajkowski discloses a desire to have an embodiment and featuring a watchdog circuit without providing details of its operation. The rejection cites paragraph [0019] of the Copending Patent Application for this proposition. The rejection states that Davis discloses a microprocessor software routine located at set microprocessor' interrupt or reset vector addresses, configured to restart the microprocessors application software. The rejection takes the position that Baylocq discloses hardening a watchdog circuit and CPU. The rejection takes the position that the references are combinable to

provide Applicants' combination and that they disclose a motivation for making the combination.

Applicants traverse this rejection. In the following sections, Applicants provide specific details as to the manner in which the art of record does not disclose particular limitations recited by Applicants and as to why the art of record, taken together, does not suggest combinations which could render Applicants' claims obvious.

The Rejection Based on the Proposed Combination

Briefly reviewing the combination rejection, the Copending Patent Application is utilized as a base reference, and the three additional references, Hosaka, Davis and Baylocq are cited as disclosing missing limitations and motivations for combination. The rejection suggests that the watchdog timer of Hosaka interacts with his microprocessor in the same manner as the recited interaction in claim 6 between Applicants' microprocessor and Applicants' hardened core circuit. Davis is cited for the disclosure of a microprocessor software routine located at the microprocessor's interrupt or reset vector addresses, configured to restart the microprocessor's application software. Baylocq is cited for the teaching of a hardened processor and watchdog circuit.

Teachings of the Patent References and the Combination

Hosaka

In the rejection, Hosaka is described as comprising an array of memory, volatile or non-volatile, connected to a microprocessor. The rejection characterizes Hosaka's watchdog timer 100 as a core circuit. The rejection states, using phraseology from claim 6 rather than from Hosaka, that Hosaka discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the hardened core circuit on a predetermined time period. The rejection further states that a core circuit is configured to read the predetermined signal from the microprocessor and activate the microprocessor's interrupt and reset control signals if the timer signal is not received within a predetermined time period. Hosaka is cited at column 2 lines 54-61 to support this proposition. While counter 80 may comprise a timer, and a form of reset signal is applied to the CPU 20, Hosaka does not produce a reset signal in the manner recited by Applicants.

For example, Claim 6, at lines 18-20, recites that a microprocessor software routine is configured to send a predetermined timer signal from the microprocessor to the hardened core circuit on a predetermined time period. This structure is explained by Applicants, for example, at paragraph [0019] and Figure 2. A timer signal 110 is generated by the microprocessor 104 software routines during a period

having a duration of T1. The timer signal 110 is routed by the microprocessor 104 to the hardened core circuit 106. The limitation in the above-cited passage of claim 6 is neither taught nor suggested by Hosaka.

At column 2, line 55 to column 3, line 2, Hosaka points out that when a program is running normally, bits are provided from the CPU 20 of a first or a second value are written into register 60 in the watchdog timer 100. The input to the register 60 reverses value at predetermined intervals of time T. This input may be seen to be a square wave, and the square wave is applied to a comparator 70 to produce another square wave at the output of the comparator 70.

Outputs of the comparator 70 are connected to a counter 80. The counter 80 counts up, but is cleared each time an input is received from the comparator 70. If inputs to the comparator 70 cease, the counter 80 continues to count up. The counter 80 requires a predetermined interval of time to count up to a preselected number. When the counter 80 reaches the preselected number, it provides an output. The output of the counter 80 is connected to provide a reset signal to the CPU 20. Therefore, if the comparator 70 does not provide an input to the counter 80 with a time interval of T', the counter 80 will produce a signal to reset the CPU 20.

The means that determine the interval in which operation of the CPU 20 must be detected, i.e., T', is provided in the watchdog timer 100 and not in the CPU 20. The CPU 20 provides a square wave output in which an interval T represents one

half cycle of the output. The output of the CPU 20 is not a timer signal defining a period within which a response to the timer signal must be produced. The CPU 20 effectively acts as a clock input for the comparator 70 and counter 80. The number of time periods T required to equal T', i.e., the time required to reach the preset count in the counter 80 is a function of the preset count in the counter 80. Thus, the time period T' is determined within the watchdog timer 100 at the counter 80. Consequently, the timing signal defining a window having a width of T' within which CPU operation must be detected is provided only by the watchdog circuit 100 and not by the microprocessor.

This is contrary to Applicants' recitations. As recited in claim 1, lines 9-12, claim 6, lines 19-21 and claim 11, lines 25-27 the timer signal is provided from the microprocessor to the hardened core circuit is connected to the microprocessor and is configured to read the timer signal from the microprocessor.

It is therefore submitted that Hosaka provides no relevant teaching for combination with the Copending Patent Application. Applicants have demonstrated a structural difference from Hosaka which is material. One consequence of this difference is that the time number of time periods T required to equal time period T' cannot be adjusted by programming of Hosaka's microprocessor. Additionally, the teachings out of Hosaka mandate the use of additional stages of circuitry not required by Applicants' recitations, e.g., the comparator 70. The additional circuitry

decreases attainable speed and reliability of the watchdog timer 100. It is therefore submitted that even assuming *arguendo* that Hosaka is properly combinable with the Copending Patent Application, the combination would not yield the apparatus as recited by Applicants.

MPEP 2143.03 requires that all limitations in the claims must be taught by the references in order to support an obviousness rejection. Since the art that is applied in combination with the Copending Patent Application, does not teach the missing limitations of Applicants' claims, it is submitted that claims 1-11 cannot be obvious in view of the art of record. It is therefore submitted that the rejection of claims 1-11 under 35 U.S.C. §103(a) and the provisional double patenting rejection should be withdrawn.

Davis

Davis is cited as disclosing a microprocessor software routine located at a microprocessor's interrupt or reset vector addresses and configured to restart the microprocessor's application software. It is submitted that Davis is not citable for this proposition. Davis at column 3, lines 55 to column 4, line 14, states that his invention provides an apparatus and method for sending a notice signal to warn a microprocessor of an impending initialization. The microprocessor is programmed to respond to complete current program tasks and to store critical data prior to the initialization. Davis discloses a means of rebooting a computer after a power

interruption after the warning signal is provided. At column 23, lines 15 - 27, Davis states that it is often desirable to interrupt power to a microprocessor in addition to toggling a state of a reset port.

The rejection suggests combining Davis for its disclosure of a software routine located at a microprocessor's interrupt or reset vector addresses configured to restart the microprocessor's application software. It is submitted that one skilled in the art would not be led to combine Davis with the two preceding references. In the above-cited passage, Davis teaches that a signal is generated to warn a microprocessor of an impending reset and to allow completion of operations. This requires that the microprocessor be operating. Both the Copending Patent Application and Hosaka generate a signal indicative of a microprocessor having become non-operational. Thus Davis solves a problem that does not exist in the art with which it is supposed to be combined. It is therefore submitted that a suggestion or motivation for the proposed combination as required by MPEP 2143.01 is not present. Therefore, Davis should not be combinable with the other art of record. It is therefore submitted that the rejection of claims 1-11 under 35 U.S.C. §103(a) and the provisional double patenting rejection on this ground should be withdrawn.

Baylocq

Baylocq is cited for the teaching of a hardened processor and watchdog circuit. It should be noted that at column 3, lines 37 - 41, Baylocq refers to a

watchdog circuit 38. The watchdog circuit 38 provides repetitions of command signals. It is not a timing or reset circuit. Baylocq states that his microprocessor 22 is radiation hardened (column 3, lines 29-30). Davis and Baylocq do not provide any teachings missing in Hosaka.

Baylocq provides for hardening of both his watchdog circuit and his microprocessor. Baylocq teaches that his microprocessor must be hardened. This is contrary to Applicants' recitations. Applicants' claims as filed recite a hardened core but do not require a hardened microprocessor. The claims as amended make it even more explicit that the microprocessor does not have to be radiation hardened. A specific recitation of, "a microprocessor not required to be radiation hardened" is made at claim 1, line 3, claim 6, line 3 and at claim 11, lines 3-4. The use of a microprocessor not required to be radiation hardened provides for the benefits of improved operation and lower cost and power requirements described above. Since the missing limitation of a microprocessor that that not have to be radiation hardened is missing, the requirement of MPEP 2143 of a showing of all elements of the combination cannot be met. It is therefore submitted that the rejection of claims 1-11 under 35 U.S.C. §103(a) and the provisional double patenting rejection on this ground should be withdrawn.

Details of the Rejections 35 U.S.C. §103(a) at Pages 10-19 of the Action

Additionally, Applicants traverse further assertions in the rejections under 35 U.S.C. §103(a). The following remarks, *inter alia,* controvert assertions in the Action beginning at page 10 thereof. These additional differences further indicate distinctions between Applicants' recitations and the teachings of the art. Each quote below is a statement from the rejection. Following each quote is Applicants' comment. In some cases, Applicants specifically point out a ground for withdrawing a rejection. In the points below where Applicants simply make a technical comment, they make the point that the suggestion in the art for combination, as required by MPEP 2143.01, is not present and that this is another factor in demonstrating that the rejections under 35 U.S.C. §103(a) should be withdrawn.

1. "As per claim 1, Hosaka discloses a computer system with improved tolerance to microprocessor functional interrupts induced by environmental sources, "

Hosaka has no teachings with respect to functional interrupts. At column 1, lines 16-36, Hosaka refers to malfunctions that may occur due to noise. This is not a teaching of functional interrupts. A functional interrupt is a form of single event effect (SEE). An SEE is an effect caused by the passage of a single ionizing particle through a microcircuit. Hosaka refers only to traditional noise effects and not to events caused by ionizing radiation.

2. Hosaka discloses a bus, "where the bus is well known to include address and data bus information, (col. 2, lines 29-30)."

At column 2, lines 29-20, Hosaka is referring to prior art which includes separate buses for data, addresses and instructions.

3. Hosaka discloses, "interrupt control, reset control, interrupt output, and power cycle output signal."

Hosaka does not refer to interrupt control. Hosaka provides only for reset. At column 1, lines 8-9 reference is made to returning a computer to its initial state. This is a reset. An interrupt goes to a selected state, but the computer does not have to "start all over." Resetting is analogous to rebooting a personal computer. This operation may take minutes, while an interrupt may occur in less than a microsecond.

5. "Hosaka further discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the said hardened core circuit on a predetermined time period (Hosaka, col. 2, lines 55-58)."

Hosaka has no teaching of hardening. Since Hosaka does not even consider functional interrupts, but only noise, Hosaka has no reason to consider hardening. The rejection is using teachings from Applicants' specification, which is not permitted

under MPEP 2143. As discussed above, the microprocessor does not send a timer signal.

6. "The core circuit [is] configured to read [a] predetermined timer signal from said microprocessor on predetermined time period and activate said microprocessor's interrupt and reset control input signals if timer signal is not received within predetermined time period to provide for removal of said microprocessor from functionally interrupted state (Hosaka, col. 3, lines 14-30 and col. 2, lines 55-58)"

The watchdog timer 100 does not receive a timer signal. It only receives pulses which constitute a square wave and act in the nature of a clock signal in that inputs from a microprocessor to a comparator result in supplying a wave with alternating levels to a counter input. The period of a timer signal is determined only in the watchdog counter. There is no interrupt disclosed in Hosaka, only reset. There is no functionally interrupted state. In columns 1 and 2, e.g., column 2, line 5, Hosaka teaches that the computer control program may run wild when noise make the computer react to data as though it were an instruction. This circumstance does not define a functionally interrupted state.

7. "It would have been obvious to one skilled in the art at the time of the invention to include the extra reset controls [of Davis] in the watchdog timer environment of Hosaka."

There is no reason suggested why Hosaka needs any extra reset controls nor what extra controls would be applied. Davis does not operate in the context of a watchdog timer. A watchdog timer watches for periods of CPU inactivity. Davis's circuit operates only when the CPU is active. MPEP 2143.01 does not permit a combination where the combination would alter the theory of operation of a base reference.

8. "Davis provides the additional improvement of providing a system that maintains critical data across reset boundaries to improve upon the time required to restore operation (Davis, col. 3, lines 5-18). This improved restoration time would obviously have furthered Hosaka's desire to reduce the amount of time the system spent in abnormal functional states."

Hosaka has no use for Davis's teachings. Hosaka's circuit resets when it determines that the processor is not operating. Davis provides a warning signal only while a computer is still operating, and then provides a reset. It is therefore submitted that Davis is not combinable with Hosaka.

9. Baylocq discloses hardening a watchdog circuit and CPU (Baylocq, col. 3, lines 40-42). It would have been obvious to one skilled in the art at the time of the invention to use the hardening of Baylocq on the watchdog circuit of Hosaka and Davis.

Baylocq does indeed disclose hardening both a watchdog circuit and a CPU. This is contrary to Applicants' recitations in each independent claim that the CPU need not be hardened. Even assuming *arguendo* that Baylocq is combinable, it does not disclose the feature of Applicants' recitations of "a microprocessor not required to be radiation hardened."

10. "It would have been obvious at the time to shield the invention of Hosaka and Davis using the hardening of Baylocq to further these goals."

Hosaka and Davis disclose no need for radiation hardened apparatus. Hosaka is concerned with traditional effects of noise in a communication link. Davis discusses effects of a power disruption. Neither Davis nor Hosaka make any reference to the effects of ionizing radiation on a microcircuit. Therefore, they have no need or desire to use more expensive, radiation hardened devices. In the hardening scheme of Baylocq, a hardened microprocessor is required. As specified above, this is contrary to Applicants' recitations.

11. "As per claim 3, Hosaka, Davis, and Baylocq further disclose the system of claim 2 further comprising a microprocessor software routine configured to read said hardened core status signal(s), and to determine if interrupt or reset activation was result of hardened core activation ... (Davis, col. 4, lines 14-25, where the activation signal causes interruption and reset). "

In the cited passage, Davis makes no reference to a hardened core or to a timer. Davis is responding to a condition occurring before cessation of operation while the recitation of claim 3 refers to operation after a computer "hang."

The Rejection Under 35 U.S.C. §112

Claims 6-10 have been rejected under 35 U.S.C. §112 in that the phrase "VLIW microprocessor" does not have an antecedent. In response to this rejection, Applicants have amended the claim 6 to remove the reference to " VLIW microprocessor." This amendment renders the recitation of microprocessor at claim 6, line 8 consistent with the recitations in claim 6 as filed at lines 3, 4, 10, 15, 16, 19 23 and 24. Applicants submit that this amendment avoids the issue. Additionally, the Examiner has objected to claim 10 as being a substantial duplicate of claim 6. Claim 10 has been amended to add "very long instruction word" prior to the recitation of VLIW and has placed VLIW in parentheses. It is submitted that the correction to claim 6 to remove the recitation "VLIW" avoids the issue as to duplication of VLIW in claim 10.

Objections to the Claims

The Examiner has objected to a number of formal errors, and has required correction. Applicants have made each of the corrections required by the Examiner. Applicants have also made further formal corrections, such as adding "the" before the recitations of certain components having antecedents.

The Rejection and of Claims 12 and 13 Under 35 U.S.C. §102

Claims 12 and 13 have been canceled to only to obviate a provisional double patenting rejection in the Copending Patent Applications. Applicants submit that this cancellation avoids issues with respect to 35 U.S.C. §102.

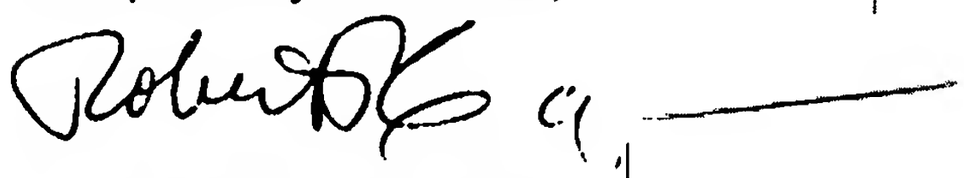
Summary

Applicants have canceled claims 12 and 13 in order to avoid a provisional statutory double patenting rejection in the Copending Patent Application. Applicants have demonstrated that the art of record does not provide the required teaching required by MPEP 2143 to support and obviousness rejection and that the cited references are not properly combinable. Applicants submit that the rejections under 35 U.S.C. §103(a) and the provisional nonstatutory double patenting rejection of claims 6-11 merit withdrawal. Formal corrections were made to obviate the rejection under 35 U.S.C. §112 and the objections to the specifications. Further formal corrections were also made. Applicant has also made amendments to claim 6, and therefore to dependent claims 7-10, as well to claim 11, to meet the rejection under 35 U.S.C. §112. Applicants assert that the cancellation of Claims 12 and 13 to obviate a provisional double patenting rejection in the Copending Patent Applications avoids any issues as to the rejection under 35 U.S.C. §102(b).

In view of the foregoing, Applicant respectfully submits that the application is now in condition for allowance. If it is believed that the application is not in condition

for allowance, the Examiner is respectfully requested to contact the undersigned to expedite the prosecution of the application.

Respectfully submitted,



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